In the Claims

Claim 1 (currently amended): A method of forming a field-effect transistor on a substrate, said method comprising steps of:

~~forming a buffer layer on said substrate, said buffer layer comprising ALD silicon dioxide;~~

utilizing a silicon tetrachloride precursor in an atomic layer deposition process to form a buffer layer on said substrate;

forming a high-k dielectric layer over said buffer layer, said high-k dielectric layer being selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide.

Claim 2 (original): The method of claim 1 further comprising a step of forming a gate electrode layer over said high-k dielectric layer.

Claim 3 (canceled).

Claim 4 (original): The method of claim 1 wherein said buffer layer comprises substantially no pin-hole defects.

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Claim 5 (original): The method of claim 1 wherein said buffer layer has a thickness less than approximately 5.0 Angstroms.

Claim 6 (original): The method of claim 2 wherein said gate electrode layer comprises polycrystalline silicon.

Claim 7 (canceled)

Claim 8 (currently amended): A method for forming a field effect transistor on a substrate, said method comprising a step of forming a buffer layer on said substrate, said method being characterized by:

utilizing a silicon tetrachloride precursor in an atomic layer deposition process to form said buffer layer on said substrate;

forming a high-k dielectric layer on said buffer layer, said high-k dielectric layer being selected from the group consisting of hafnium oxide, zirconium oxide, and aluminum oxide~~ wherein said buffer layer comprises ALD silicon dioxide~~.

Claim 9 (original): The method of claim 8 further comprising a step of forming a gate electrode layer over said high-k dielectric layer.

Claim 10 (canceled)

Claim 11 (original): The method of claim 8 wherein said buffer layer comprises substantially no pin-hole defects.

Claim 12 (original): The method of claim 8 wherein said buffer layer has a thickness less than approximately 5.0 Angstroms.

Claim 13 (original): The method of claim 9 wherein said gate electrode layer comprises polycrystalline silicon.

Claims 14-20 (canceled)

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